REMARKS

Claims 1-20 are pending, with Claims 1 and 6 being independent. Claims 1 and 6 been amended. No new matter has been added. Reconsideration and allowance of the above-referenced application are respectfully requested.

The Abstract has been amended to reduce the number of words to within the range of 50 to 150.

Rejections Under 35 U.S.C. §103(a)

Claims 1-8, 11-12 and 16 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,062,124 issued to Hayashi et al. (hereinafter "Hayashi") in view of U.S. Patent No. 6,791,987 issued to Eng et al. (hereinafter "Eng").

Claims 5, 9-10, 13-15 and 17-20 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Hayashi in view of Eng and further in view U.S. Patent No. 5,846,248 issued to Rokugo (hereinafter "Rokugo"). These contentions are respectfully traversed.

Initially, it appears that the Examiner has misunderstood Hayashi and Eng, and contrary to the Examiner's contention, the combination of Hayashi and Eng would not result in the claimed

invention. Not only was there no motivation to combine Hayashi with Eng at the time of the invention; in fact, the teaching of Hayashi appears to be incompatible with the teaching of Eng.

The subject matter as claimed in amended Claims 1 and 6 is a system and method for transmitting data from a source module to a terminating module over a network comprising a plurality of modules in which each of the modules in the network operate with an independent clock. The terminating module is synchronized to the clock of the source module using the accumulated phase difference, which is transmitted over the network to the terminating module. The accumulated phase difference is the difference between the input and output of each of the modules through which the data is transmitted. The terminating module receives all the accumulated phases differences and uses them to lock an output clock with the input clock of the source module.

Hayashi discloses a system for synchronizing the master clock of a first communication system with a reference clock supplied by a signal from an external communication system. Within the first communication system there is a master clock, so that each module within the communication system is synchronized with other modules. When the first communication system is connected to an outside data network it receives data that uses a reference clock, which is different from the master clock of the first communication system. Thus, the system

described in Hayashi is used to synchronize the master clock of the first communication system with the reference clock received from the external network.

This is accomplished by the device I1, which is connected to the external network calculating a phase difference between the reference clock from the external network and the master clock of the first communication system. This calculated phase difference is sent to device I2, which contains the master clock oscillator. The master clock oscillator is then adjusted based on the phase difference received from device I1 to match the phase of the reference clock.

It is clear that in the system of Hayashi each of the modules within the communications system are synchronized with each other as they use the same master clock. The inputs and outputs of each module are also synchronized with the master clock. It is only the input from the external network that is not synchronized initially. However, subsequent to adjustment of the master clock all of the inputs and outputs of the communication system are synchronized with one another.

In sharp contrast, amended Claim 1 requires that each of the modules in a network have outputs that are not synchronized with the input to the module. That is clearly not the case in the system disclosed in Hayashi. Claim 1 also requires that each module in the network operates with a clock that is not

synchronized with the clocks of the other modules in the network. Again, this is clearly not the case in Hayashi. Claim 1 also requires determining a phase difference between the input clock and the output clock of each module (and there are a plurality of them) and transmitting that accumulated phase difference to the terminating module in the network. Again that is clearly not disclosed in Hayashi.

Eng discloses a system which allows for the synchronization of the clocks of two communication systems, A and B by counting the arrival of packets sent from system A at system B over time. Systems A and B communicate over a network (see Figure 4) but no phase difference information of the modules in the network is calculated and sent to the terminating module in system B. The synchronization of system B with system A is accomplished simply by monitoring the average rate of packet arrivals at system B to approximate the transmission rate of system A. There is no accumulated phase difference information transmitted over the network.

Combination of Hayashi and Eng

As noted above, the teaching of Hayashi would simply not have been combined with the teaching of Eng in the manner alleged by the Examiner. Hayashi relates to synchronizing the master clock of a synchronized network with a reference clock of an external data signal. Eng relates to synchronizing the clock

of a receiving system B with the clock of a transmitting system A, where the two systems are connected over an asynchronous network. These are two very different problems. It is difficult to see how the teaching of Eng could be applied to the system of Hayashi.

Furthermore, even if Hayashi and Eng could be combined (which is not conceded by the Applicant), the combination of Hayashi and Eng would still not result in the claimed invention. For example, neither Hayashi nor Eng discloses the feature of transmitting an accumulated phase difference between the input clock and the output clock of each of a plurality of modules in a network that connects a source module to a terminating module.

Granted, Hayashi does calculate a phase difference between a reference clock and a master clock of a synchronized system and passes that phase difference back to the master clock so that it can be adjusted. However, that is not the same thing as having a plurality of modules in an asynchronous network each passing the phase difference between their input and their output to a terminating module so that the terminating module can calculate a phase difference between its clock and a source module. The system of Hayashi is provided simply to avoid the need for an additional communications line between the external network connection and the master clock of a synchronous

communications system. Ultimately, in the system of Hayashi, all of the modules in the network are synchronized. This is precisely what the subject matter of claim 1 avoids.

Eng does appear to relate to the same sort of problem that the claimed invention addresses, but provides a completely different type of solution, which does not require any timing information from the asynchronous network over which the data is transmitted. The system of Eng is only applicable to constant bit rate traffic.

Thus, neither Hayashi nor Eng teaches or suggests all the features of independent Claim 1. Therefore, the proposed Hayashi-Eng combination does not teach or suggest each and every limitation of Claim 1 and Claim 1 should be in condition for allowance.

Independent Claim 6 recites similar features as Claim 1 and is also patentably distinguishable over the proposed Hayashi-Eng combination for analogous reasons to those discussed for independent Claim 1.

Additionally, Claims 2-5, 7-8, 11-12 and 16 depend generally from independent Claims 1 or 6; these dependent claims are patentably distinguishable over Hayashi or Eng, either alone or in combination, for at least the reasons provided above.

Furthermore, Claims 5, 9-10, 13-15 and 17-20 also depend generally from independent Claims 1 or 6; these dependent claims are patentably distinguishable over Hayashi, Eng, or Rokugo, either alone or in combination, for at least the reasons provided above.

In addition, many dependent claims are allowable for additional reasons. For example, in relation to Claim 3, Hayashi does not use two counters (43 and 48) simultaneously. The selector 102 selects the input of one or the other. In relation to Claim 4, there is no mention in Hayashi or in Eng of using a lower frequency clock to latch the count of a higher frequency clock.

Thus, all the pending claims are allowable for at least the reasons provided above.

The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, the above arguments for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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/Cheng C. Ko/
Cheng C. Ko
Reg. No. 54,227

Fish & Richardson P.C.
PTO Customer No. 20985
12390 El Camino Real
San Diego, California 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10799643.doc